Fig. 5 has been objected to as not corresponding with the specification at page 10, lines 14 and 17 which name reference signal 512. The specification has been amended to delete reference signal 512 as this reference signal is not necessary for the understanding of Figure 5. Reference signal 512 is used to identify the computer system of Figure 5. The specification clearly states that a Figure 5 is an illustration of a computer system, therefore identification of the computer system by reference signal 512 is not necessary. Therefore, Figure 5 now corresponds with the specification.

Specification

The specification has been objected to for various reasons. Specifically, the title of the invention is not descriptive. Applicants amended the title of the invention in the preliminary amendment to read "SYSTEM AND DEVICE INCLUDING A BARRIER LAYER." Applicants fail to see how this title is not descriptive of the claimed invention and in compliance with MPEP §606.01.

The abstract has been objected to as being unclear. The abstract has been amended to clarify and correspond with the claims of the present invention.

The specification has been objected to for failing to contain the reference signal 407 shown in Fig. 4. As stated above, a new Fig. 4 is being submitted with this paper. New Fig. 4 contains the appropriate reference sign 401 in place of the inappropriate reference sign 407. Therefore, reference signal 407 is no longer shown in Fig. 4. Fig. 4 now corresponds with the specification.

The specification has been objected to as failing to provide antecedent basis for the "source rail" recited in claim 31. The specification has been amended to provide basis for the "source rail" as recited in claim 31 as filed.

Applicants have checked the application and have made other corrections, by amendment, where necessary. No new matter has been added for any of the amendment to the specification.

Rejection under §102

Claim 30 has been rejected under 35 USC § 102(e) as being anticipated by Lee et al. (U.S. Patent No. 6,218,260). Lee et al. teaches a method of forming integrated circuit capacitors having improved electrode and dielectric capacitors. A diffusion barrier layer is formed on the lower electrode and then a dielectric layer is formed over the diffusion barrier layer. The diffusion barrier layer is formed by a first layer of silicon nitride using a rapid thermal nitridation process and then forming a second layer of silicon nitride on the first layer using a CVD method. The first layer of silicon nitride may be formed by applying a compound gas at a high temperature to the surface layer. See col. 10, lines 56-64.

Claim 30, as amended, recites a primarily nitride silicon-containing barrier layer comprising a silicon-containing material, from a precursor layer previously deposited over at least a portion of the first electrode, that has been reacted with a nitridizing agent. There is no mention of a barrier layer comprising these elements in Lee et al. Rather, Lee et al. teaches a barrier layer formed through chemical vapor deposition (CVD). Lee et al. also teaches that the barrier layer can be formed by using rapid thermal nitridation (RTN). When using the CVD process as described by Lee et al., the silicon is reacted with the nitrogen while simultaneously being deposited to form the layer of silicon nitride. Thus, there is no precursor layer that is deposited before reaction with the nitrogen containing ambient takes place. When the RTN process of Lee et al. is used, silicon from the underlying conductive doped HSG layer is used to form the barrier layer, not a precursor layer containing silicon as claimed. Therefore, every element of claim 30 is not recited and claim 30 is not anticipated by Lee et al. Furthermore, Lee et al. does not suggest or mention a precursor layer that is reacted with a nitridizing agent for the barrier layer. Therefore, claim 30 is patentable over Lee et al.

Rejection under §103

Claim 31 has been rejected under 35 USC §103(a) as being unpatentable over Hu (U.S. Patent No. 5,962,904) in view of Mills et al. (U.S. Patent No. 5,696,917). Hu teaches a method of making a gate electrode stack with a diffusion barrier. A layer of silicon-containing material is positioned above the gate oxide layer. See col. 3, line 61-62. A diffusion barrier is then formed over and in contact with the layer of silicon-containing material. See col. 4, lines 1-8. The barrier comprises electrically conductive silicon material, preferably a refractory metal. See col. 4, lines 2-8.

Mills et al. teaches in Fig. 2 and at col. 9, lines 24-30, a system 200 having a microprocessor 210, a high speed bus 220, a low speed bus 260, a bus bridge 280 and a flash memory 230. The microprocessor 210 is coupled to the memory 230 and SRAM 240 by the high speed bus 220. The bus bridge 220 couples the high speed bus 280 to the low speed bus 260.

The Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect Hu's device to the computer system taught by Mills et al. Hu teaches a method of making a gate electrode stack wherein the diffusion barrier is a refractory metal silicon nitride layer. However, Hu does not mention a barrier layer that comprises a precursor layer that is reacted with a reactive agent in order to form the barrier layer. Hu does teach positioning a silicon-containing material over a gate oxide layer, then forming a diffusion barrier that is made of a refractory metal silicon nitride layer over the silicon-containing material. The structure is exposed to a heating process, however, this heating process is to the already formed barrier layer not to a precursor layer containing silicon. Hu teaches exposing the barrier layer to the heating process to illustrate that the electrically conductive silicon nitride material of the barrier is self-passivating in that it does not significantly oxidize during the oxidation process. This prevents the formation of silicides in the electrically conductive material that will reduce the conductivity of the gate electrode stack. There is no teaching or suggestion of a silicon-containing barrier layer deposited over the first oxide layer comprising a silicon-containing material in a precursor layer, previously deposited over a portion of a first electrode, that has been reacted with a reactive agent. Mills et al. does not cure this

deficiency as Mills et al. does not teach or suggest the formation of a barrier layer in a memory device.

Therefore, if the device of Hu was connected to the computer system taught by Mills et al., claim 31, as amended, would not result. Rather, the result would be a memory device in a computer system having is a refractory metal silicide barrier layer formed over a gate oxide layer. This barrier layer, once formed, is exposed to a heating process. This is not the invention as recited in claim 31, as amended. Therefore, claim 31, as amended, is nonobivous and patentable over Hu in view of Mills et al.

New claims 32-60 all recite, or ultimately depend from claims that recite, a silicon-containing material, previously deposited, that is reacted a reactive agent to form a barrier layer. This structure is not taught or suggested in the cited prior art. Thus, claims 32-60 are patentable.

In CONCLUSION

Applicants respectfully submit that, in view of the above amendments and remarks, the application is now in condition for allowance. Early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
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Appendix

Please amend the Cross-References to Related Applications to read:

CROSS-REFERENCES TO RELATED APPLICATIONS

This application is related to commonly assigned U.S. Patent Application Serial Nos.: [_/___,___]09/653,096 [(Attorney Docket No. MIO0060PA)], METHOD FOR FORMING A DIELECTRIC LAYER TO INCREASE SEMICONDUCTOR DEVICE PERFORMANCE, [__]filed August 31, 2000, by Powell et al. and [_/___,___]09/653,298 [(Attorney Docket No. MIO0061)], METHOD FOR FORMING A DIELECTRIC LAYER AT A LOW TEMPERATURE, [_____]filed August 31, 2000, by Mercaldi et al., the disclosures of which are incorporated herein by reference.

At page 10, lines 14-23, the please amend the paragraph as follows:

Figure 5 is an illustration of a computer system [512] that can use and be used with embodiments of the present invention. As will be appreciated by those skilled in the art, the computer system [512] would include ROM 514, mass memory 516, peripheral devices 518, and I/O devices 520 in communication with a microprocessor 522 via a data bus 524 or another suitable data communication path. The mass memory 516 can include silicon-containing barrier layers in, for example, transistor structures or charge storage structures. The mass memory 516 may further include a substrate, a drain, a source rail, and an oxide layer. Generally, the drain and source rail are formed in the substrate. The oxide layer is typically deposited over the substrate and stretches from the drain to the source rail. The silicon-containing barrier is generally deposited over the first oxide layer. These devices can be fabricated according [with] to the various embodiments of the present invention.

Please amend the Abstract on page 23 to read:

ABSTRACT OF THE DISCLOSURE

[Methods] Systems and devices are disclosed utilizing a silicon-containing barrier layer. [A method of forming a barrier layer on a semiconductor device is disclosed. A semiconductor

device is provided. A silicon-containing material is deposited on the semiconductor device. The silicon-containing material is processed in a reactive ambient. The barrier layer can be made primarily oxide, primarily nitride or both by the reactive ambient selected.] A semiconductor device is disclosed[. The semiconductor device] and includes a substrate, a gate oxide, a silicon-containing barrier layer and a gate electrode. The gate oxide is formed over the substrate. The silicon-containing barrier layer is formed over the gate oxide by causing silicon atoms of a precursor layer react with a reactive agent. The gate electrode is formed over the silicon-containing barrier layer. [Other embodiments utilizing a barrier layer are disclosed.]

In the Claims

30. (Amended) A capacitor device comprising:

a first electrode formed over a substrate;

a primarily nitride silicon-containing barrier layer [formed over the electrode] on said first electrode, said barrier layer comprising a silicon-containing material from a precursor layer, previously deposited over at least a portion of said first electrode, that has been reacted with a nitridizing agent;

a dielectric layer formed over the primarily nitride silicon-containing barrier layer; and

a second electrode formed over the dielectric layer.

31. (Amended) A computer system comprising:

at least one processor;

a system bus;

a memory device coupled to the system bus, the memory device including one or more memory cells comprising:

a substrate;

a drain formed in the substrate;

a source rail formed in the substrate;

a first oxide layer deposited over the substrate stretching from the drain to the source rail;

a silicon-containing barrier layer deposited over the first oxide layer said barrier layer comprising a silicon-containing material from a precursor layer, previously deposited over at least a portion of said first electrode, that has been reacted with a reactive agent; and

a gate electrode deposited over the silicon-containing barrier layer.

32. (New) A device comprising:

a substrate including at least one semiconductor layer;

a semiconductor device fabricated proximate to the substrate; and

a barrier layer formed from a silicon source previously deposited over at least a portion of the semiconductor device, having been reacted with a reactive agent.

33. (New) The device of claim 32, wherein the silicon source is a silazane.

34. (New) The device of claim 32, wherein the silicon source is selected from the group comprising hexamethyldisilazane, tetramethyldisilazane, octamethylcyclotetrasilazine, hexamethylcyclotrisilazine, diethylaminotrimethylsilane and dimethylaminotrimethylsilane.

35. (New) The device of claim 32, wherein the silicon-containing material is from a silane source.

36. (New) The device of claim 32, wherein the reactive agent is selected from the group comprising NH_3, N_2, O_2, O_3, N_2O and NO.

37. (New) The device of claim 32, wherein the barrier layer is primarily nitride.

38. (New) The device of claim 32, wherein the barrier layer is primarily oxide.

39. (New) The device of claim 32, wherein the barrier layer is primarily oxynitride.

40. (New) A device having a barrier layer comprising:

a substrate including at least one semiconductor layer;

a first semiconductor device fabricated proximate to said substrate;

a silicon-containing material, previously formed over at least a portion of said first semiconductor device, that has been reacted with a reactive agent to form a barrier layer; and

a second semiconductor device formed over said barrier layer.

41. (New) The method of claim 40, wherein the reactive agent is NH_3 and the barrier layer is primarily nitride.

42. (New) A device having a barrier layer comprising:

a silicon substrate including at least one semiconductor layer;

a silicon-containing material from a silazane source, previously formed over at least a portion of said silicon substrate, that has been reacted with a reactive ambient to form said barrier layer.

43. (New) A semiconductor device having a barrier layer comprising:

a substrate having at least one semiconductor layer:

a transistor structure formed proximate to said substrate, said transistor structure including

a source formed in said substrate,

a drain formed in said substrate, and

a gate oxide layer formed over an active area between said source and drain; and

a silicon-containing material, previously formed over at least a portion of the transistor structure, that has been reacted with a reactive agent to form the barrier layer.

44. (New) The device of claim 43 wherein a gate electrode is formed over said barrier layer.

45. (New) The device of claim 43, wherein said gate electrode is doped with phosphor.

46. (New) The device of claim 43, wherein said gate electrode is doped with boron.

47. (New) The device of claim 43, wherein said reactive agent comprises an oxidizing agent which causes silicon atoms of the silicon-containing material to bond with oxygen atoms of the oxidizing agent.

48. (New) A capacitor device comprising:

an electrode formed over a substrate;

a silicon-containing material, from a precursor layer previously formed over the electrode, that has been processed using rapid thermal nitridation with a nitridizing reactant to form a barrier layer; and

a dielectric layer formed over said barrier layer.

49. (New) A semiconductor device having a barrier layer containing no metal comprising:

a substrate including at least one semiconductor layer; and

a silicon-containing material, from a silicon source previously formed over at least a portion of the semiconductor device, that has been reacted with a reactive agent to form said barrier layer containing no metal.

50. (New) A semiconductor device having a barrier layer containing no metal comprising:

a silicon substrate including at least one semiconductor layer; and

a silicon-containing material, from a silazane source previously formed over at least a portion of the silicon substrate, that has been reacted with a reactive agent to form said barrier layer containing no metal.

51. (New) A semiconductor device having a barrier layer containing no metal comprising:

a substrate having at least one semiconductor layer;

a transistor structure formed proximate to said substrate, said transistor structure including:

a source formed in said substrate,

a drain formed in said substrate, and

a gate oxide layer formed over an active area between said source and drain; and

a silicon-containing material, previously formed over at least a portion of the transistor structure, that has been reacted with a reactive agent to form said barrier layer containing no metal.

52. (New) A capacitor device with a barrier layer containing no metal comprising:

an electrode formed over a substrate;

a silicon-containing material, previously formed over said electrode, wherein said silicon-containing material has been processed using rapid thermal nitridation with a nitridizing reactant to form the barrier layer containing no metal; and

a dielectric layer formed over said barrier layer.

53. (New) A capacitor device comprising:

a first electrode formed over a substrate;

a silicon-containing barrier layer formed over at least a portion of said first electrode, said barrier layer comprising a silicon-containing material from a precursor layer previously deposited over at least a portion of said first electrode from a silicon source, reacted with a reactive agent selected to react with silicon of the silicon-containing material;

a dielectric layer formed over said silicon-containing barrier layer; and

a second electrode formed over the dielectric layer.

54. (New) The capacitor device of claim 53, wherein the silicon source is a silazane.

55. (New) The capacitor device of claim 53, wherein the silicon source is selected from the group comprising hexamethyldisilazane, tetramethyldisilazane, octamethylcyclotetrasilazine, hexamethylcyclotrisilazine, diethylaminotrimethylsilane and dimethylaminotrimethylsilane.

56. (New) The capacitor device of claim 53, wherein the silicon-containing material is from a silane source.

57. (New) The capacitor device of claim 53, wherein the reactive agent is selected from the group comprising NH_3, N_2, O_2, O_3, N_2O and NO.

58. (New) The capacitor device of claim 53, wherein the barrier layer is primarily nitride.

59. (New) The capacitor device of claim 53, wherein the barrier layer is primarily oxide.

60. (New) The capacitor device of claim 53, wherein the barrier layer is primarily oxynitride.